REMARKS

Claims 1-30 were originally submitted.

Claims 9, 10, and 22 were previously canceled.

Claim 24 was previously amended.

Claims 31-38 were added in a previous response.

Claims 1-8, 11-21, and 23-38 remain in this application.

Cited References

All of the submitted claims were rejected in the Office Action of November 18, 2003 based upon a single reference: US Patent 6,590,781 to Kollipara et al (hereinafter referred to as "Kollipara").

Kollipara describes an apparatus that includes a plurality of memory circuits arranged on a module. The apparatus allows a clock signal to be generated and to travel through the connected modules and through the memory circuits of those modules. This allows a clock loop to be formed. *See abstract of Kollipara.*

The memory circuits may be placed on either or both sides of a module. When the memory circuits are placed on both sides of the module, an internal bus connects the memory circuits to allow a clock signal to travel between the memory circuits. The bus extends from a first set of edge fingers at a first edge of the module, traverses the entire first primary surface of the module, folds back at an opposite second edge of the module, traverses the entire second primary surface of the module, and terminates at a second set of edge fingers at the first edge. *See Fig. 2, and col. 4, lines 21-28 of Kollipara.*

Multiple modules may be connected with one another with fl xible connectors. In effect the connectors connect the busses and memory circuits of the modules. Connectors are provided at a particular edge of the module, since the module busses loop back to that particular edge as discussed above. *See Fig. 15A of Kollipara.*

To provide for a clock loop, it is desirable to maintain a continuous bus loop when multiple modules are connected. Therefore Kollipara particularly provides busses that loop back when connecting memory modules and may be arranged such that when modules are connected that clock loop continuity is maintained.

The claimed invention recites particular language that channels (busses) extend across a substrate (module) from one edge to an opposite edge, and contacts at the opposite edges to allow communications through the channel. Contrast this with Kollipara that describes a bus (channel) that originates at one edge and terminates at the same edge in order to provide a continuous loop. Further contrast the bus in Kollipara that provides for a clock signal, not communications.

Because of Kollipara's intent to provide a continuous clock loop the arrangement of channels (busses) extended from one edge to the opposite edge of a substrate is not described, since such an arrangement may terminate the clock loop that connects the memory devices in Kollipara. Furthermore, the busses described in Kollipara are particularly intended for clock signals not communications.

35 U.S.C. §102

Claims 1, 4-8, 11-14, 19-21, 23-29, 31-34 and 37-38 are rejected under 35 U.S.C. §102(e) as being anticipated by Kollipara. Applicants respectfully traverse the rejection.

Independent claim 1 recites

> An apparatus comprising:
>
> a substrate having first and second opposite edges;
>
> a plurality of memory devices disposed on the substrate;
>
> a plurality of channels extending between the opposite edges, wherein each of the plurality of memory devices is coupled to one of the plurality of channels; and
>
> electrical contacts at the opposite edges of the substrate configured to allow communications through the channels via the electrical contacts.

Kollipara does not disclose or suggest a "plurality of channels extending between the opposite edges". Kollipara describes channels (busses) that loop back to one edge of a substrate or module, or channel that are arranged to connect adjacent edges of a module; however, Kollipara does not show channels that extend from one edge to an opposite edge of a substrate. *See Fig. 15 A of Kollipara.*

The Examiner cites Fig. 15A of Kollipara as disclosing a plurality of channels that extend between the opposite edges (of the substrate), and electrical contacts at the opposite edges of the substrate configured to allow communications. Column 9, lines 4-9 are particularly pointed out as reciting electrical contacts at the opposite edges.

As shown in 15A, the only edge of a module (substrate) 152a having electrical contacts is the edge connected at flexible connector 154. The opposite edge of module 152a is connected to connector 151a; however, Kollipara does not disclose or suggest that electrical contacts exist at this edge. Connector 151a is a physical connector, not an electrical connector. If channels do extend between the opposite edges and electrical contacts are provided at the opposite edges, electrical contacts would be available at the edge placed on connector 151a.

Kollipara describes a bus or channel that begins at an originating edge, traverses the substrate and loops back to the originating edge maintaining a continuous clock loop. *See Fig. 2 of Kollipara.* If the channels did extend across the substrate and electrical contacts were provided at the edge attached to connector 154 and the edge attached to connector 151a, the clock loop would terminate, defeating the intent of Kollipara.

Other configurations described in Kollipara provide that the busses be bent or angled such that connections may be made at adjacent edges to maintain clock loop continuity. *See Figs. 12A, 12B, 12C, 13A, 13B, 13C, 13D, and 15B of Kollipara.* Kollipara does not disclose or suggest that channels extend from one edge to an opposite edge.

Further, claim 1 recites "electrical contacts at the opposite edges of the substrate configured to allow communications through the channels." Kollipara's busses provide for clock signals and not communications such as data to be passed between the circuits.

For at least these reasons, Kollipara does not suggest the elements of claim 1. Accordingly, the rejection of claim 1 is improper, and should be withdrawn.

Dependent claims 4-6 depend from and comprise all the elements of claim 1. As such, dependent claims 4-6 are allowable by virtue of their dependency on base claim 1. Applicants respectfully request that the §102 rejection of claims 4-6 be withdrawn.

Independent claim 7 recites similar language as claim 1. Claim 7 in part recites:

> a first substrate having a plurality of memory devices disposed thereon and a first channel portion extending across the first substrate, the first substrate having opposite ends and contacts at the opposite ends to allow communications through the first channel portion via the contacts at the opposite ends of the first substrate;
>
> a second substrate having a plurality of memory devices disposed thereon and a second channel portion extending across the second substrate, the second substrate having opposite ends and contacts at the opposite ends to allow communications through the second channel portion via the contacts at the opposite ends of the second substrate

The Examiner rejects claim 7 based on the same arguments as claim 1 citing Kollipara. Applicants reassert the arguments above supporting claim 1 and particularly that Kollipara does not disclose or suggest channels that extend across a substrate to opposite ends with contacts at the opposite ends to allow communication.

For at least these reasons, Kollipara does not suggest the elements of claim 7. Accordingly, the rejection of claim 7 is improper, and should be withdrawn.

Dependent claims 8, 11-14, and 19-20 depend from and comprise all the elements of claim 7. As such, dependent claims 8, 11-14, and 19-20 are allowable by virtue of their dependency on base claim 7. Applicants respectfully request that the §102 rejection of claims 8, 11-14, and 19-20 be withdrawn.

Independent claim 21 recites similar language as claims 1 and 7. Claim 21 in part recites:

> a first memory module having contacts at opposite ends thereof, a first channel portion extending across the first memory module between the contacts;
>
> a second memory module having contacts at opposite ends thereof, a second channel portion extending across the second memory module between the contacts;

The Examiner rejects claim 21 based on the same arguments as claims 1 and 7 citing Kollipara. Applicants reassert the arguments above supporting claim 1 and particularly that Kollipara does not disclose or suggest contacts at opposite ends and channel portions that extended across a memory module between contacts.

For at least these reasons, Kollipara does not suggest the elements of claim 21. Accordingly, the rejection of claim 21 is improper, and should be withdrawn.

Dependent claim 23 depends from and comprises all the elements of claim 21. As such, dependent claim 23 is allowable by virtue of its dependency on base claim 21. Applicants respectfully request that the §102 rejection of claim 23 be withdrawn.

Independent claim 24 recites similar language as claims 1, 7, and 21. Claim 24 in part recites:

> arranging channel portions on a substrate such that the channel portions extend between opposite edges of the substrate;
>
> arranging contacts at the opposite edges of the substrate to allow communication between the contacts at the opposite edges through the channel portions;

The Examiner rejects claim 24 based on the same arguments as claims 1, 7 and 21 citing Kollipara. Applicants reassert the arguments above supporting claim 1 and particularly that Kollipara does not disclose or suggest channel portions on a substrate that extend between opposite edges of the substrate and contacts at the opposite edges of the substrate to allow communication between the contacts at the opposite edges.

For at least these reasons, Kollipara does not suggest the elements of claim 24. Accordingly, the rejection of claim 24 is improper, and should be withdrawn.

Dependent claims 25-29 depend from and comprise all the elements of claim 24. As such, dependent claims 25-29 are allowable by virtue of their dependency on base claim 24. Applicants respectfully request that the §102 rejection of claims 25-29 be withdrawn.

Independent claim 31 recites similar language as claims 1, 7, 21 and 24. Claim 31 in part recites:

> each of the first and second memory modules having contacts at first and second opposite ends thereof and having one or more communication channel portions extending between the contacts;

The Examiner rejects claim 31 based on the same arguments as claims 1, 7, 21 and 24 citing Kollipara. Applicants reassert the arguments above supporting claim 1 and particularly that Kollipara does not disclose or suggest contacts at first and second opposite ends of a memory module and having one or more communication channel portions extending between the contacts.

For at least these reasons, Kollipara does not suggest the elements of claim 24. Accordingly, the rejection of claim 24 is improper, and should be withdrawn.

Dependent claims 32-34 and 37-38 depend from and comprise all the elements of claim 31. As such, dependent claims 32-34 and 37-38 are allowable by virtue of their dependency on base claim 31. Applicants respectfully request that the §102 rejection of claims 32-34 and 37-38 be withdrawn.

35 U.S.C. §103

Claims 2, 3, 15-18, 30, 35, and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kollipara. Applicants respectfully traverse the rejection.

Dependent claims 2 and 3 depend from and comprise all the elements of claim 1. As such, dependent claims 2 and 3 are allowable by virtue of their dependency on base claim 1.

Kollipara does not teach or suggest "a plurality of channels extending between the opposite edges" as recited by claim 1. As discussed above, Kollipara describes busses that either loop from a first edge to the opposite edge and back to the first edge, or are angled to travel from one adjacent edge to another.

Further, Kollipara does not teach or suggest "communications through the channels". As discussed above, Kollipara describes busses for clock signals and does not teach or suggest that such busses may be used for communications.

The Examiner argues that Kollipara teaches "a memory module including a substrate having a first and second side[s] with the plurality of channel conductors disposed on both sides thereof" as further recited by claims 2 and 3. Applicants do not disagree with the Examiner as to Kollipara teaching a substrate with first and second sides; however, applicants do not agree that Kollipara teaches that the channel conductors are disposed on both sides. As discussed above, Kollipara describes a single bus that is looped internally in a memory module and connects

the memory circuits on either side of the memory module. Separate channel conductors are not disposed on both sides, since Kollipara intends to maintain a continuous clock loop.

Accordingly, claims 2 and 3 are allowable for at least the reasons discussed. Applicants respectfully request that the §103 rejection of claims 2 and 3 be withdrawn.

Dependent claims 35 and 36 depend from and comprise all the elements of claim 31. As such, dependent claims 35 and 36 are allowable by virtue of their dependency on base claim 31.

The Examiner rejects claim 35 and 36 based on the same arguments as claim 31. Applicants reassert the arguments above supporting claim 31, and particularly as discussed above that Kollipara does not teach or suggest that the channel conductors are disposed on both sides.

Accordingly, claims 35 and 36 are allowable for at least the reasons discussed. Applicants respectfully request that the §103 rejection of claims 35 and 36 be withdrawn.

Dependent claims 15-18 depend from and comprise all the elements of claim 7. As such, dependent claims 15-18 are allowable by virtue of their dependency on base claim 7.

In particular Kollipara does not disclose or suggest channels that extend across a substrate to opposite ends with contacts at the opposite ends to allow communication as recited by claim 7. As discussed above the bus described in Kollipara is internally routed from one edge of a memory module to an opposite edge and loops back to the originating edge, allowing clock signals to travel to and from memory circuits that are placed on either side of the memory module. The

bus does not extend across the opposite ends (edges) and provides contacts on the opposite ends to allow communication.

Accordingly, claims 15-18 are allowable for at least the reasons discussed. Applicants respectfully request that the §103 rejection of claims 15-18 be withdrawn.

Dependent claim 29 depends from and comprises all the elements of claim 24. As such, dependent claim 29 is allowable by virtue of their dependency on base claim 24.

In particular Kollipara does not disclose or suggest channel portions on a substrate that extend between opposite edges of the substrate and contacts at the opposite edges of the substrate to allow communication between the contacts at the opposite edges as recited in claim 24.

Accordingly, claims 15-18 are allowable for at least the reasons discussed. Applicants respectfully request that the §103 rejection of claims 15-18 be withdrawn.

Conclusion

It is respectfully submitted that all claims are in a condition for allowance, and action to that end is requested. The Examiner is requested to telephone the undersigned if that would be helpful in expediting allowance.

Respectfully Submitted,

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By: _____

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